ABSTRACT

A data processing chip with a flexible timing system and method for supplying clocks to a digital data processing system useful for power conservation. A phase locked loop generates a master clock from which a core clock and a system clock are derived. The frequency of each of the core and system clocks is independently controllable relative to the master clock and can be changed on the fly with glitch free and jitter free operation. The data processing chip is well suited for use in hand held electronic devices where power management is a concern. Power can be saved by lowering the frequency of the core clock, even for short intervals of time.